Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1-5. (Cancelled)

6. (Currently Amended) A Viterbi decoding device with a dual-data input and a dual-data output, comprising:

a branch metric calculating circuit performing branch metric calculation operations on two consecutive input data according to two sets of target levels, respectively, to obtain a plurality of branch metric values, wherein said two sets of target levels are ~~different from each other~~ obtained via a partial response channel PR(1,1,1,1) and are (-2,-1,0,1,2) and (-1.5,-1,0,1,1.5);

an adder-comparator-selector unit coupled to said branch metric calculating circuit, performing accumulative additional operations of said branch metric values to obtain four groups of accumulated values, respectively, comparing said accumulated values in groups, and outputting two control signals and four least accumulated values according to the comparing results;

a metric register unit coupled to said adder-comparator-selector unit, receiving and storing said four least accumulated values, and feeding back said four least accumulated values to said adder-comparator-selector unit to perform next accumulative addition operations;

a survivor memory unit coupled to said adder-comparator-selector unit, recording a plurality of output-data state transition tracks in response to said two control signals; and

a decision unit coupled to said metric register unit and said survivor memory unit, determining the combination of the two probable output-data state transition tracks as said consecutive output data according to said four least accumulated values.

7. (Original) The Viterbi decoding device according to claim 6 further comprising a normalizing circuit coupled to said adder-comparator-selector unit and said metric register unit, performing a normalized shift when said least accumulated values exceed the threshold value.

8. (Original) The Viterbi decoding device according to claim 6 wherein said adder-comparator-selector unit comprises:

a plurality of accumulators coupled to said branch metric calculating circuit, performing accumulative operations of said plurality of branch metric values for said plurality of output-data state transition tracks, respectively;

two comparators coupled to said plurality of accumulators, comparing two of said four groups of accumulated values so as to output said two control signals, respectively; and

two selectors coupled to said plurality of accumulators, said two comparators and said metric register unit, outputting said four least accumulated values that stored in said metric register unit in response to said two control signals, respectively.

9. (Original) The Viterbi decoding device according to claim 6 wherein said metric register unit includes four registers.

10. (Original) The Viterbi decoding device according to claim 6 wherein said survivor memory unit comprises a plurality of memories coupled in series.

11. (Original) The Viterbi decoding device according to claim 6 wherein said plurality of output-data state transition tracks are determined according to a 3T run-length limited algorithm.

12. (Cancelled).

13. (Cancelled).

14. (Currently Amended) A Viterbi decoding method with a multi-data input into a multi-data output, comprising of:

providing ~~a plurality of target level sets, wherein said target level sets are different from one another~~ two target level sets obtained via a partial response channel PR(1,1,1,1) which are (-2,-1,0,1,2) and (-1.5,-1,0,1,1.5), respectively;

performing branch metric calculating operations of a plurality of consecutive input data according to said ~~plurality of~~ two target level sets to obtain a plurality of branch metric values, respectively;

performing accumulative additional operations of said branch metric values to obtain a plurality of accumulated values, respectively, comparing said plurality of accumulated values in groups, and outputting a plurality of control signals and a plurality of least accumulated values according to the comparing results;

storing said plurality of least accumulated values, and feeding back said plurality of least accumulated values to said adder-comparator-selector unit to perform next accumulative additional operations; and

recording a plurality of output-data state transition tracks in response to said control signals, and determining the combinations of a plurality of probable output-data state transition tracks as said consecutive output data according to said least accumulated values, wherein said plurality of output-data state transition tracks are determined according to a 3T run-length limited algorithm and wherein said consecutive input data and said consecutive output data are two-bit input and two-bit output, and eight output-data state transition tracks are recorded.

15. (Original) The Viterbi decoding method according to claim 14, further comprising performing a normalized shift said least accumulated values exceed the threshold value.

16-19. (Cancelled).